Abstract of the Disclosure

A protocol processor for processing first header information of a reception packet to provide instructions for processing second header data of a reception packet is provided. For efficient protocol processing, special hardware architectures are necessary. Hardware architectures for dynamic length input buffer, no penalty conditional jump, one clock-cycle case-based jump, accumulated partial comparison, and integrated layer processing on-the-fly are described. The architectures are used in a domain-specific protocol processor, which is based on program controlled execution. The processor does not operate on data stored in a memory, but on an incoming packet-flow with constant speed. The processor performs every instruction in one clock-cycle, including conditional jump (taken and not taken) and case based jump.